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INDUCTIVE COUPLED PLASMA ETCHING OF HIGH ASPECT RATIO SILICON CARBIDE MICROCHANNELS FOR LOCALIZED COOLING

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ABSTRACT

High aspect ratio microchannels using high thermal conductivity materials such as silicon carbide (SiC) have recently been explored to locally cool micro-scale power electronics that are prone to on-chip hot spot generation. Analytical and finite element modeling shows that microchannels used for localized cooling should have high aspect ratio features (above 8:1) to enable the heat flux levels required to locally cool GaN transistors to temperatures below 100°C. This work presents experimental results of microfabricating high aspect ratio microchannels in a 4H-SiC substrate. Depths of 90 and 80 µm were achieved with a 5:1 and 12:1 aspect ratio, respectively. This microfabrication process used to create high aspect ratio features in SiC will enable the integration of microchannels (backside features) with high-power density devices such as GaN-on-SiC based electronics, as well as other SiC-based microfluidic applications.

INTRODUCTION

Gallium nitride (GaN) transistors used in high power and high frequency electronics generate power densities as high as 10 W/mm of channel width leading to temperature rises as high as 200°C which can decrease reliability [1–3]. Therefore, it is important to reduce the peak temperatures of these hot spots to increase operation lifetime. Silicon carbide (SiC) substrates are often used in the design of GaN-based electronics due to its high thermal conductivity (370 W/m-K) which can be leveraged to reduced device channel temperatures. However, the use of SiC alone is not sufficient to reduce the channel temperatures as the thermal conductivity of SiC drastically reduces with an increase in temperature [4]. Thus, the addition of microchannels and cooling fluid into the SiC substrate is one solution for decreasing device temperatures during operation. This approach allows the use of both convective and conductive heat transfer to reduce overall temperature of the system and increases the overall heat flux of the system and local cooling [5]. It is approximated that channel temperatures can remain below 110°C using this integrated cooling architecture [6].

Silicon based microchannel heat exchangers have been demonstrated in the past with various geometries to optimize thermal cooling [7–11]. However, Si thermal conductivity is low the growth of power devices on Si substrates results in increased leakage currents due to the generation of thin film defects. Therefore, SiC substrates, although costly, have been identified for the development of SiC-based and GaN-based power electronics devices. However, the plasma etching of SiC often results in slow etch rates (0.2 µm/min to 1 µm/min) and reduced selectivity in comparison to well established plasma etches for Si substrates. Previous work in plasma etching of SiC has primarily focused mainly on the manufacturing of large via holes and feature sizes greater than 50 µm [12]. However there are reports of 10 µm width trenches with depths of 110 µm, creating a 11:1 aspect ratio [13] and trench widths of 13 µm and 7.6:1 aspect ratio in 6H-SiC [14]. However, there is little reported on smaller opening widths and large depths (higher aspect ratios) in 4H-SiC.

This paper presents analytical calculations of high aspect ratio SiC performance and experimental results in the fabrication of high aspect SiC microchannels. First the analytical

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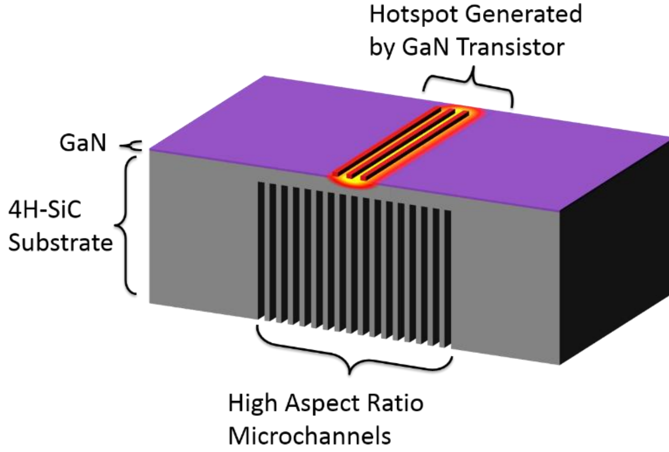

Figure 2. Schematic illustration of high aspect ratio 4H-SiC trenches used for localized cooling of hot spots generated by high power operation of GaN transistors.

calculation of high aspect ratio SiC microchannels efficiency is presented. Next, a finite element model is presented to approximate expected hotspot temperatures for a hotspot source. Next, parameters for plasma etch conditions are investigated to assist in the realization of deep, high aspect ratio microtrenches in SiC. Finally, a gallery of SEM images of microchannels with varied depth, density, and aspect ratio are presented. The fabrication of these high aspect ratio microchannels could be used in the future integration of backside microchannel cooling of hot spots generated by high power density devices (Figure 1) to reduce on-chip temperatures and improve device reliability.

FIN EFFICIENCY ANALYSIS

Fin efficiency is a common metric to analyze microchannel arrays used in thermal management applications. We analyzed four fin array geometries that were fabricated in bulk 4H-SiC in Table 1, which are presented later in this paper. Fin efficiency is assumed for rectangular, long channels using. The efficiency of a single fin is commonly known to be [15]:

$$\eta_{fin} = \frac{\tanh(mL)}{mL} \tag{1}$$

Where L is the length of the fin plus half the fin thickness, and m refers to:

$$m = \left(\frac{2h}{kt}\right)^{1/2} \tag{2}$$

Where h is the heat transfer coefficient, t is the fin thickness, and k is the thermal conductivity of the SiC substrate.

Table 1 Summary of SiC microchannel dimensions fabricated and analyzed with fin efficiency calculations. Device surface cooling area is assumed constant at 1.5 μm long, so number of fins varies.

Channel #	Channel Depth	Channel Width	Fin Width	Channel Aspect Ratio	# Fins
1	47 μm	8.5 μm	10 μm	5:1	81
2	38 μm	4.5 μm	19.5 μm	8:1	62
3	58 μm	4.7 μm	21.5 μm	12:1	57
4	90 μm	20 μm	20 μm	4:1	37

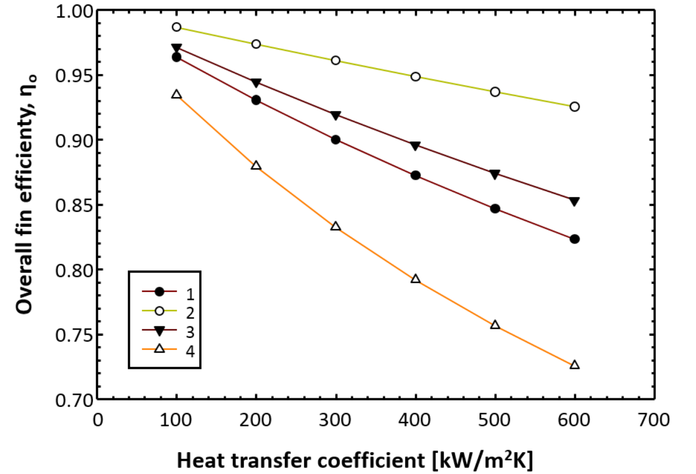

Figure 1. Analytical analysis of fin efficiency for the various geometries summarized in Table 1. The legend labels refer to the Channel # in Table 1.

And the overall fin efficiency of an array of microchannels is expressed as:

$$\eta_o = 1 - \frac{NA_{fin}}{A_{total}}(1 - n_{fin}) \tag{3}$$

Where A_{fin} refers to the surface area of one fin, N is the number of fins and channels, and A_{total}, the total surface area of the heat exchanger, can be expressed as a function of fin spacing g and A_{fin}:

$$\eta_o = 1 - \frac{NA_{fin}}{N(A_{fin}+g)}(1 - n_{fin}) \tag{4}$$

Thus, it becomes clear that smaller spacing between fins, and thus smaller microchannels, leads to higher fin efficiency, and thus higher improvement in thermal cooling. Figure 2 shows the results from the fin efficiency calculations for the

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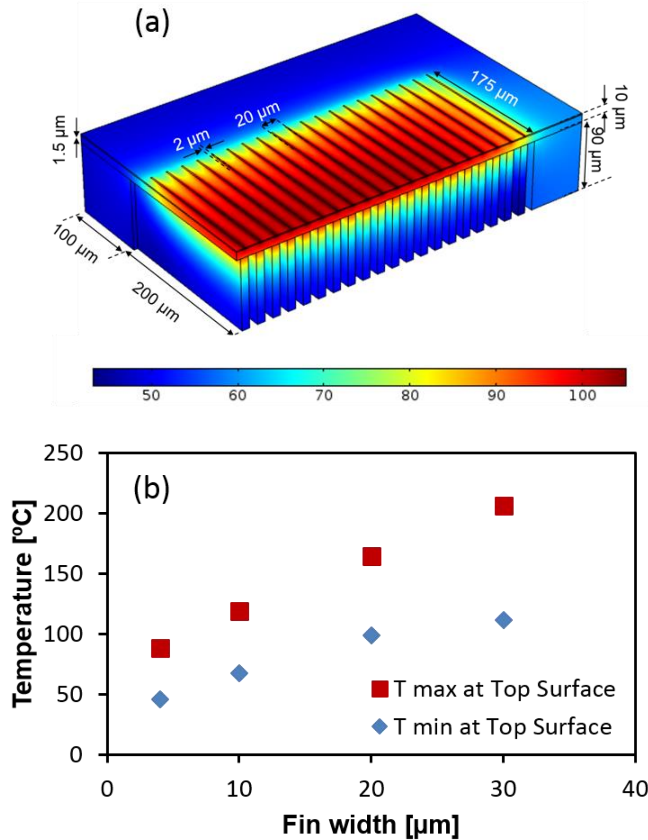

Figure 3 (a) An example of the conduction simulation result using 3D COMSOL Multiphysics. The color map shows the temperature distribution of SiC heat exchanger with a power to the system of 50 W and heat transfer coefficient of 450 kW/m^2· K. The fin width is 10 µm and fin pitch is 20 µm. (b) Hot spot temperature (maximum and minimum) variation with respect to fin width for an array of GaN HEMTs being cooled with SiC microchannels.

microchannel geometries summarized in Table 1. The numerical results show that higher aspect ratio channels have larger fin efficiency, and fin thickness and channel depth also play important roles in the overall fin efficiency. Overall fin efficiencies were evaluated for an appropriate range of constant heat transfer coefficients, h = 100 to 600 kW/m^2·K which were obtained from both single-phase conjugate computational fluid dynamic (CFD) simulations and relevant two-phase boiling correlations for four specific channel configurations in **Error! Reference source not found.** using methanol as a working fluid [5].

HOT SPOT TEMPERATURE COMPUTATION

A simulation was performed using COMSOL Multiphysics software to account for the thermal resistances associated with the heat source, spreader, and heat exchanger. COMSOL Multiphysics software solves for the temperature field as the solution to the steady state heat conduction equation. The device

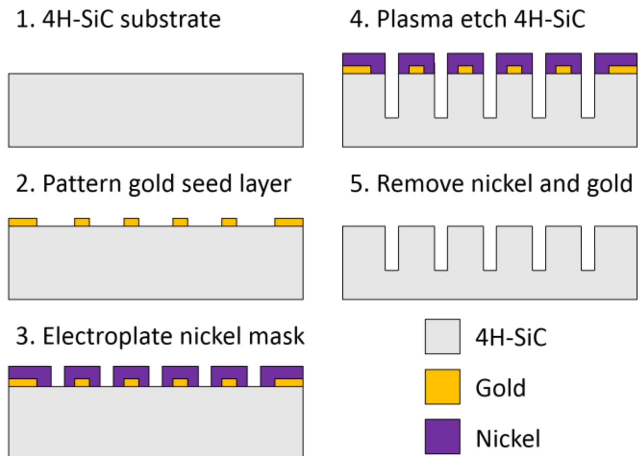

Figure 4. Microfabrication process used to manufacture high aspect ratio SiC microchannels using an electroplated Ni mask.

in the simulations include 1 µm GaN, 10 µm SiC substrate, and 90 µm height SiC fin (See Figure 3a). An array of 20 transistor gates in the quarter device is modeled as the hot spot generator. As boundary conditions, heat fluxes are given to the gates (2 µm x 175 µm x 20 in the quarter device). A constant heat transfer coefficient of 400 kW/m^2·K is imposed to the fin walls. Symmetry boundary conditions are used to account for the quarter device. The inlet temperature is 25°C. The simulation accounts for the material properties and device dimensions for each layer to solve the conduction equations where the thermal conductivity of GaN and SiC is the function of temperature.

Figure 3 compares the junction temperature with varying fin width. Here we impose a constant heat transfer coefficient to understand of the effect of surface area to volume ratio. In reality, the effective heat transfer coefficient is larger for a smaller channel, which will improve the impact of small hydraulic diameter Thus, finite element modeling has confirmed that smaller channel and fin widths leads to lower hot spot temperatures, thus improved cooling of the device hot spots.

SIC MICROCHANNEL FABRICATION PROCESS

The predicted increase in fin efficiency and decrease in hotspot temperature with respect to high aspect ratio SiC channels justified the experimental fabrication microchannels in 4H-SiC. Microchannels were fabricated using 4H-SiC substrate (Cree Inc. supplier, high purity semi-insulating, >1E5 ohm-cm, double side polished). Dies of 1 cm by 1cm were used for experiments due to the high cost of SiC substrates. The SiC underwent a piranha clean (H_2SO_4:H_2O_2, 9:1), then rinsed in deionized water and acetone, methanol, and isopropanol. Next a standard 1:1 contact photolithography process was used to pattern photoresist.

For etch characterization experiments, a 200 nm Ni film was evaporated and patterned using a lift-off process. The SiC was

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then etched using PlasmaTherm's LL-ICP Metal Etch system with a baseline recipe of 1000 W ICP power, 100 W RF bias power, 5 mTorr chamber pressure, and 9:1 ratio of SF_6/O_2 gas chemistry, and a total flow rate of 60 sccm. The RF bias power was varied between 25 W and 200 W to characterize etch rate and SiC:Ni selectivity. The etch rate was also characterized with varied pressure between 4.7 and 10 mTorr. Each 10 minute etch was measured using a stylus-based profilometer (Alphastep 500) on a 1 mm by 1 mm etch area. The etch selectivity of SiC:Ni was measured using a ratio of SiC etch rate with respect to Ni etch rate. The Ni mask was measured before the SiC etch. The step height measured after the SiC etch, and then the Ni mask was removed and the sample re-measured to calculate the final thickness of the mask. The difference between these etch depths gives the measurement of Ni mask removed, and thus the Ni etch rate.

For long, high aspect ratio microchannels (summarized in Figure 4), a 50 nm gold film was evaporated and patterned using a lift-off process. Nickel was then electroplated using a Watt's bath chemistry [16] to create a >1.5 μm thick Ni hard mask. The SiC was then etched using the baseline recipe and 50 W RF bias power. Since narrow trench openings require a longer etch rate [17], these samples were etched for 2.5 hours and 4 hours to reach depths from 50 to 100 μm.

PLASMA ETCH CHARACTERIZATION RESULTS

To obtain high aspect ratio channels, it is important to first characterize the etch rates of the plasma chamber with respect to varied RF bias power and chamber pressure. A high SiC:Ni selectivity is desired in addition to high SiC etch rate. Figure 5a shows a high SiC:Ni selectivity at 100 W RF bias power, and an etch rate around 0.6 μm/min. However lower bias powers can be used to reduce undesired artifacts such as redeposited Ni, which causes micromasking pillars, as seen in Figure 6. Additionally, Figure 4b shows higher etch rates at lower pressures, so 5 mTorr was chosen for the high aspect ratio etch.

Higher pressures (10 mTorr) can also lead to higher etch rates due to higher plasma density, but this should be further investigated for limits in the high aspect ratio regime. The limits of mass transport in narrow areas [18] may require lower pressure etching.

The opening in mask size (i.e. aspect ratio) also affects the etch rate of the substrate. Figure 6 shows the effect of varied aspect ratio on the overall depth of the microchannel. Narrower openings result in a reduced etch rate.

There are additional etching artifacts that result in SiC etching. First, the micromasking effect due to the sputtering and redeposition of Ni [18] causes grass-like structures in large open area etching. At etch openings lower than 10 microns, no micromasking is observed. Additionally, sidewall roughness is another challenge that appears in microchannels. Organic polymer also deposits on the sidewall during etching, and is another source of micromasking and stringing. Finally, additionally sidewall ion bombardment can lead to additional depth at the corner of trenches, a phenomena referred to as micro-trenching.

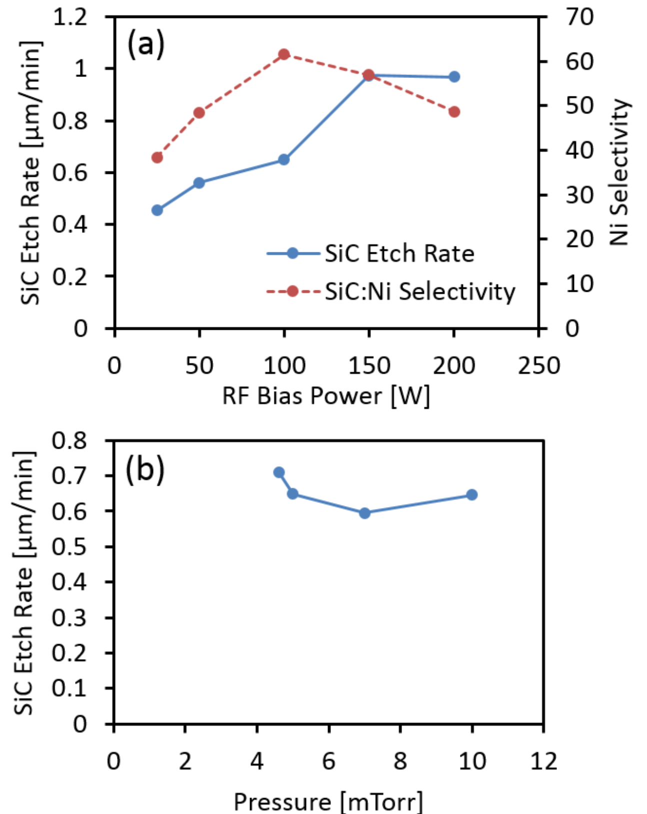

Figure 5. SiC etch rate with respect to varying plasma parameters. (a) SiC etch rate with respect to RF bias power and (b) SiC etch rate respect to chamber pressure. The baseline plasma etch parameters used are ICP power = 1000 W, RF Bias power = 100 W, chamber pressure = 5 mTorr, and O_2/SF_6 ratio of 10% and flow rate of 60 sccm.

HIGH ASPECT RATIO SIC MICROCHANNEL RESULTS

This process was used to investigate narrow microchannels with varying opening widths between 4 and 100 μm microchannels. The varied aspect rato microchannels shown in Figure 6 show aspect ratio dependant etch dephs, etching artifacts, and furthermore, aspect ratio dependant microtrench results. Higher aspect ratios (> 9:1) show a convergence of the microtrench effects to a narrow and tapered channel. Additionally, this effect appears in repeated trenches of microchannel arrays, showin in Figure 7. High aspect ratio channels > 12:1, Figure 7 a, have narrower width at the bottom of the channel versus the top opening. This is due to limits of etching at deeper aspect ratios. As the channel gets deeper, the etch rate decreases due to limited mass transport of the plasma gas to the bottom of the narrow trench. Finally, narrow channels also show some variation in directionality in the evolution of the channel. The limits of the plasma gas transport into the channel

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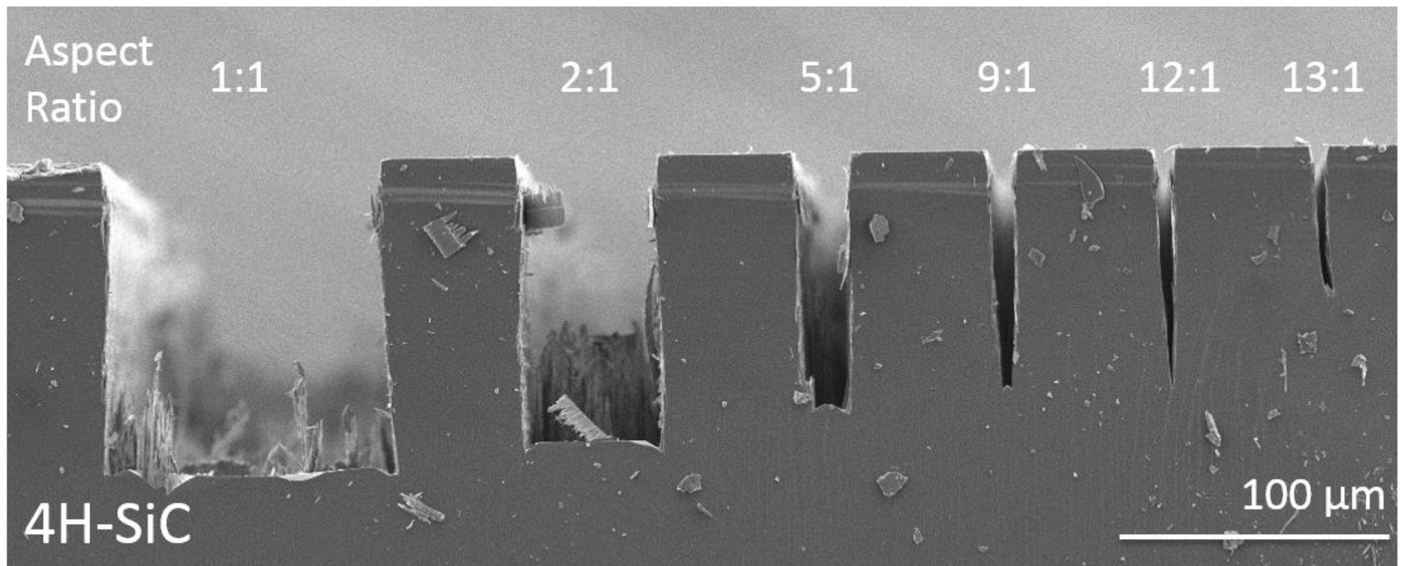

Figure 6. SEM image of plasma etched SiC microchannels with various mask opening widths.

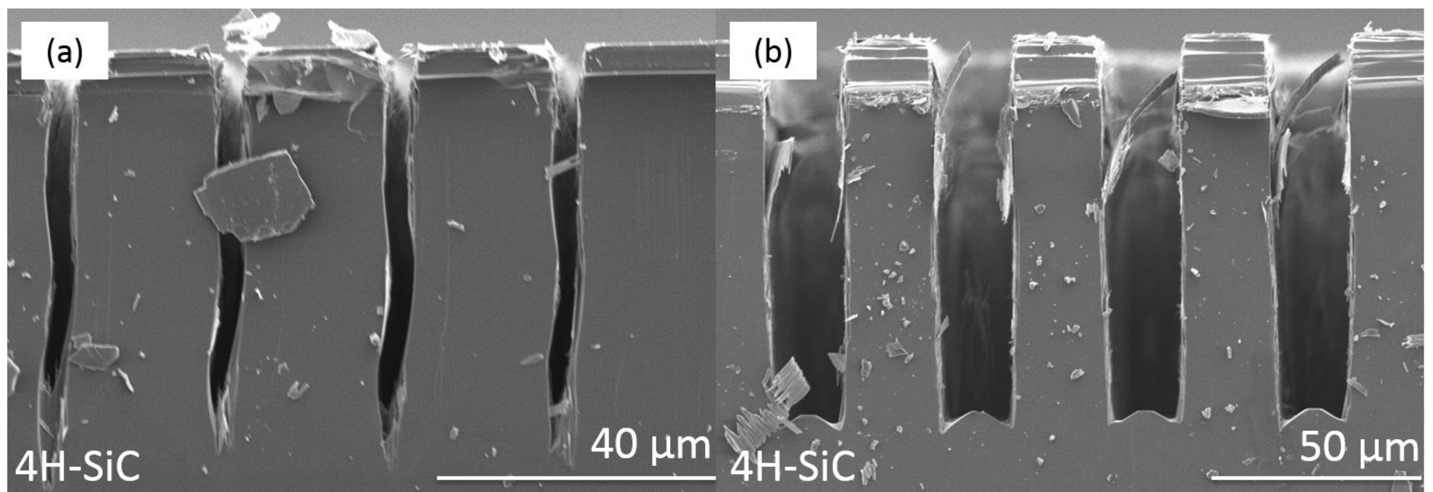

Figure 7. SEM images of high aspect ratio SiC microchannels. (a) High aspect ratio SiC channels (12:1) with narrow opening widths (4.7 µm) have reduced etch depth and thinning profiles. (b) Wide channels (20 µm) have lower aspect ratio channels (4:1) and show microtrenches at channel corners.

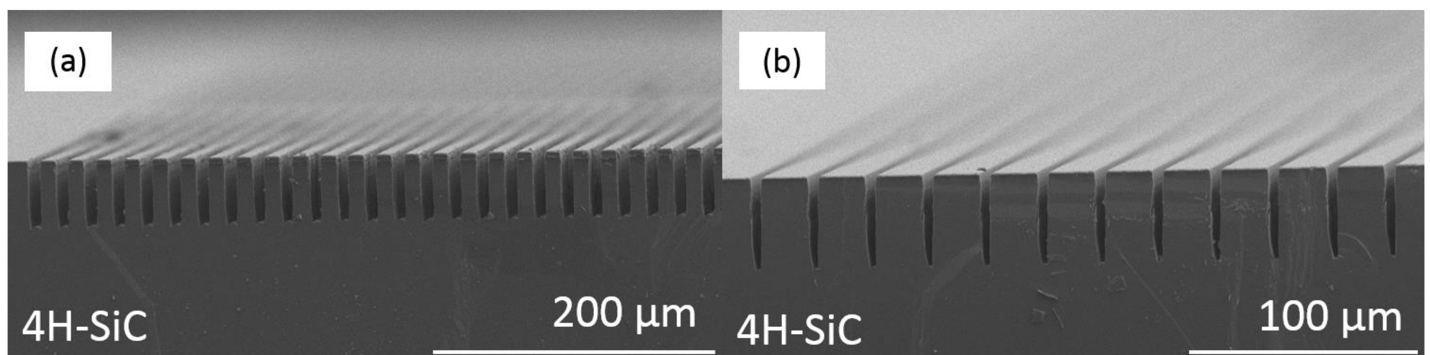

Figure 8. SEM images of high density arrays of high aspect ratio SiC microchannels. (a) 8.5 µm wide, 47 µm deep microchannels with aspect ratio of 5:1 and (b) 4.5 µm wide, 38 µm deep microchannels with aspect ratio of 8:1.

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cause greater directional variation. Smaller variations in plasma etching are amplified due to the narrow spacing.

Large arrays of microchannels have been implemented using the developed etching processes studied here. Figure 8a shows an array of 25 microchannels that are 47 µm deep, 800 µm long, with an aspect ratio of 5:1. These channels show high similarity in shape, depth, and overall appearance. An array of 12 high aspect ratio channels (8:1) are shown in Figure 8b are 38 µm deep and >1000 µm long.

CONCLUSION

This work demonstrated the fabrication of high aspect ratio microchannels in 4H-SiC for microcooling of hot spots. The fin efficiency increases for high aspect ratio fins and microchannels. Additionally, finite element computation was used to show the reduction in surface hot spot temperature with decreased fin and channel width. We created microchannels with aspect ratios varying from 1:1 to 13:1 with depths of 110 µm to 51 µm, respectively. Finally, we created high density arrays of over 20 microchannels with aspect ratios of 5:1 and 12 microchannels with aspect ratios of 8:2. These results could be implemented in a convective heat exchanger for the cooling of high power GaN and SiC electronic applications.

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