# Thermal Interface Resistance Measurements for GaN-on-Diamond Composite Substrates

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*Abstract* — **The performance of high-power gallium nitride (GaN) high-electron-mobility transistors (HEMTs) is limited by self-heating effects. High thermal resistances within micrometers of the active device junction often dominate the junction temperature rise and fundamentally limit the device power handling capability. The use of high-thermal-conductivity diamond in close proximity to the transistor junction can mitigate this thermal constraint, but careful attention is required to the quality of the thermal interface between the GaN and diamond. Here we apply time-domain thermoreflectance (TDTR) to two GaN-on-diamond composite substrates with varying GaN thicknesses to measure the thermal interface resistance between the GaN and diamond (29 m$^2$ K GW$^{-1}$) as well as the thermal conductivity of the GaN buffer layer (112 W m$^{-1}$ K$^{-1}$) at room temperature. Informed by these data, we perform finite-element analysis to quantify the relative impact of the GaN-diamond thermal interface resistance, diamond substrate thermal conductivity, and a convective cooling solution on the device channel temperature rise.**

*Keywords* — **High-Electron-Mobility Transistors (HEMT), Gallium Nitride (GaN), Diamond, Thermal Boundary Resistance (TBR), Thermal Interface Resistance, Thermal Conductivity, Time-Domain Thermoreflectance (TDTR), Electronics Cooling**

## I. INTRODUCTION

Gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) are promising for high-power electronic applications such as a radar amplifier [1]. High electrical breakdown fields of GaN and high electron charge densities at the AlGaN/GaN heterojunction enable higher-power and higher-frequency operation of GaN-based transistors than GaAs- and Si-based transistors allow [2], [3]. However, device-level self-heating and associated thermal management challenges at this higher power density severely limit the peak power density and impair the device reliability [4], [5]. High thermal resistances in the “near-junction” region (i.e., a region within micrometers of the heated electronic junction) often hinder efficient heat transport from the active device regions to the heat sink components [4], [6], [7]. Since the spreading resistance of the substrate makes a key contribution to the overall thermal resistance of the devices, the selection of a suitable substrate material is crucial [7].

SiC has been a common choice as a substrate material due to its higher thermal conductivity (~400 W m$^{-1}$ K$^{-1}$) than that of Si (~142 W m$^{-1}$ K$^{-1}$) and sapphire (~35 W m$^{-1}$ K$^{-1}$) [7]. But the near-junction thermal resistance of GaN-on-SiC devices still restricts efficient heat spreading away from the active device regions and therefore limits the device performance and reliability [4], [8]. The integration of chemical-vapor-deposited (CVD) diamond substrate in close proximity to the transistor junction holds promise in improving the near-junction cooling of GaN HEMT devices mainly due to its excellent heat spreading capability. A typical value for the room-temperature thermal conductivity of high-quality polycrystalline CVD diamond is near 1500 W m$^{-1}$ K$^{-1}$ [9], which is higher by a factor of nearly 5 than that of SiC. However, the large mismatch of key crystalline properties (i.e., lattice constants and coefficients of thermal expansion) of GaN and diamond compared to the mismatch of these properties of GaN and SiC creates a challenge for the fabrication of high-quality GaN on diamond substrate [10], [11].

Current GaN-on-diamond fabrication technologies can be grouped broadly into two categories: i) direct GaN heteroepitaxy on single crystalline diamond [11]-[13] and ii) GaN epilayer transfer to polycrystalline CVD diamond [8], [14]-[16]. The former method involves approximately 1-μm-thick transition layers between the GaN and single crystal diamond for strain compensation. Such relatively thick transition layers often contain high densities of defects, and exhibit high thermal resistance [15]. The second method, used in this work, involves the transfer of pre-grown AlGaN/GaN heterostructures to polycrystalline CVD diamond using a thin intermediate adhesion layer (~50 nm). This approach is beneficial in that the thermal resistance of the intermediate material between the GaN and diamond is much lower than that of the first approach. But this approach still requires reduction in the thermal interface resistance between the GaN and diamond.

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In this paper, we use time-domain thermoreflectance (TDTR) to extract the thermal conductivity of the GaN buffer layer as well as the GaN-diamond thermal interface resistance for two GaN-on-diamond composite substrates with varying GaN thicknesses. Our data suggest that the GaN/diamond thermal interface resistance is near 30 $m^2$ K $GW^{-1}$ at room temperature for the current GaN-on-diamond composite substrates. Informed by our data and other available literature data, we perform finite element thermal analysis to quantify the relative impact of the GaN-diamond thermal interface resistance as well as other resistance components on the device channel temperature rise (see Appendix).

## II. Samples and Experimental Methods

Figure 1 shows the two GaN-on-diamond composite substrates used in this study, with two different GaN thicknesses (0.85 µm and 0.37 µm). The AlGaN/GaN heteroepitaxial layers are first grown on a Si substrate by metal-organic chemical vapor deposition (MOCVD). The material stack consists of an ~25-nm-thick GaN/AlGaN device layer, an ~0.8-µm-thick GaN buffer layer, and an ~1-µm-thick AlN and AlGaN transition layer on top of the Si substrate. The 1-µm-thick transition layer serves to reduce lattice mismatch stresses during growth. Because it is highly resistive [15], we etch it as well as the Si substrate away. Then, an ~30-nm-thick disordered adhesion layer is deposited on the back-side of the GaN buffer layer, and CVD diamond with a thickness of approximately 100 µm is grown on top of the adhesion layer. Two composite substrates with this final structure are fabricated; one remains as it is and the other is etched to a different GaN thickness of 0.37 µm. The two samples are coated with a thin Al film of ~47 nm that acts as the temperature transducer for TDTR measurements.

Cross-plane thermal conductivity of the GaN buffer layer and thermal interface resistance between the GaN and the diamond are measured by TDTR. TDTR is a well-established technique used to measure thin film thermal conductivities and thermal interface resistances in multi-layer stacks [17]-[22]. Details of our TDTR setup are described in [21] and [22]. We fit the TDTR data with three parameters: the Al/GaN thermal boundary resistances (TBRs) $R_{b,\,Al\text{-}GaN}$ , the thermal conductivity of the GaN buffer layer $k_{GaN}$ , and the GaN-diamond thermal interface resistance, $R_{b,\,GaN\text{-}Diam}$ . The GaN-diamond thermal interface resistance is not the discrete boundary resistance but rather involves multiple resistance contributions: i) the thermal resistance of low-quality GaN regions near the adhesion/diamond interface, ii) the two discrete boundary resistances at the adhesion layer interfaces with the GaN and the diamond, iii) the intrinsic thermal resistance of the adhesion layer, and iv) the thermal resistance of the near-interfacial diamond (i.e., the nucleation/coalescence regions). These resistance contributions are lumped and represented as a single effective interface resistance. We use literature values for the heat capacities of the constituent layers [9], [23], [24], and we assume a range of thermal conductivity from 400 W $m^{-1}$ $K^{-1}$ to 2000 W $m^{-1}$ $K^{-1}$ for the thermal conductivity of the diamond substrate [9]. The diamond thermal conductivity within the assumed range has a minimal impact on the fitted values of $k_{GaN}$ and $R_{b,\,GaN\text{-}Diam}$ [25].

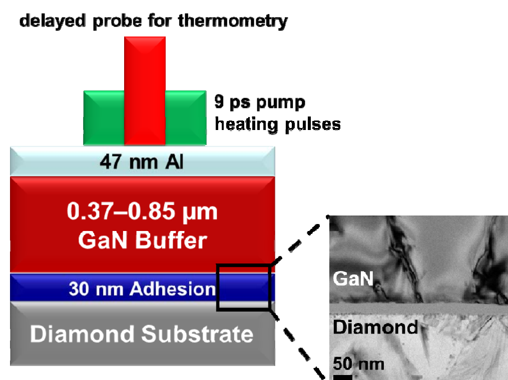


Fig. 1. Cross-sectional schematic drawing of the GaN-on-diamond composite substrates used in this study with a representative cross-sectional transmission electron micrograph near the GaN-diamond interface.

## III. Results and Discussion

Figure 2a shows representative TDTR data with the best analytical fits at room temperature for the two GaN-on-diamond composite substrates. We simultaneously fit the TDTR data from the two samples under the assumption that $k_{GaN}$ and $R_{b,\,GaN\text{-}Diam}$ do not vary strongly between the two samples [22], [26]. Using this approach, we find $k_{GaN}$ = 112 ± 15 W $m^{-1}$ $K^{-1}$ and $R_{b,\,GaN\text{-}Diam}$ = 29 ± 2 $m^2$ K $GW^{-1}$ at room temperature. The uncertainty in the values is due to variations in the thickness of the Al transducer film (47 ± 2 nm). The room-temperature Al/GaN thermal boundary resistance is determined to be 13 $m^2$ K $GW^{-1}$ for the thicker GaN sample and 10 $m^2$ K $GW^{-1}$ for the thinner GaN sample.

Our approach takes advantage of different measurement sensitivities to these two properties at different GaN thicknesses [22]. We define a TDTR sensitivity coefficient as the logarithmic derivative of the thermoreflectance signal $R$ with respect to the thermal

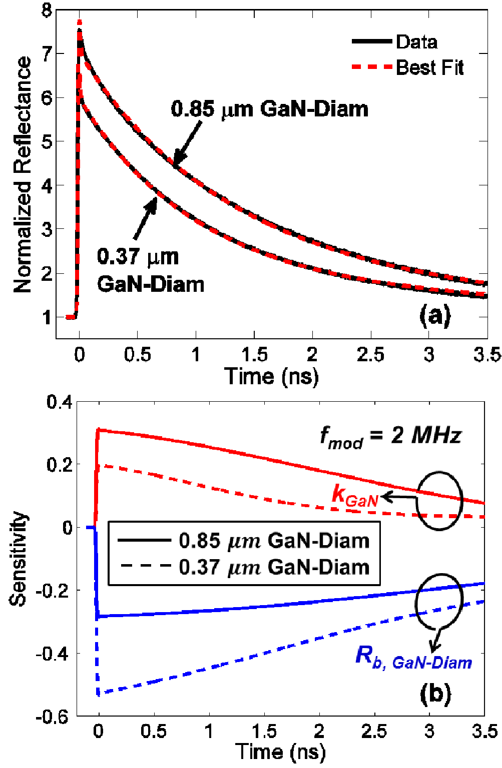


Fig. 2. (a) Representative TDTR data (black solid lines) with best analytical fits (red dashed line) for the two GaN-on-diamond composite substrates. (b) Sensitivity coefficients for the GaN thermal conductivity (red lines) and the GaN-diamond thermal interface resistance (blue lines) for the two samples as a function of the pump-probe delay time.

parameter of interest $\alpha$ : $S_\alpha = \partial \ln(R) / \partial \ln(\alpha)$ . Figure 2b illustrates the sensitivity coefficients for $k_{GaN}$ and $R_{b,\ GaN\text{-}Diam}$ for the two different thickness samples and as a function of the probe delay time. The thicker GaN sample primarily affects the value of $k_{GaN}$ whereas the thinner GaN sample mostly determines the value of $R_{b,\ GaN\text{-}Diam}$.

The GaN thermal conductivity determined here is lower than the values found previously [7], [22], [26], which can be attributed to the size effect as well as the effect of phonon scattering on material defects. The GaN-diamond thermal interface resistance determined here is also lower than what we measured previously [15] mainly due to the absence of the highly resistive transition layer. Our measured interface resistance is comparable to the recent Raman-measured value of 27 $m^2$ K $GW^{-1}$ at approximately 400 K [16].

## V. CONCLUSIONS

We extract the GaN-diamond thermal interface resistance as well as the thermal conductivity of the GaN buffer layer using TDTR on two GaN thicknesses. Recent simulation [7] has shown that a GaN-on-diamond configuration with an interface resistance of below 30 $m^2$ K $GW^{-1}$ can outperform a GaN-on-SiC configuration even with zero interface resistance in terms of the device channel temperature rise. The interface resistance of the current GaN-on-diamond composite substrates seems to reach this target. With an anticipated reduction in the interface resistance, the GaN-on-diamond composite substrates should enhance the near-junction cooling of HEMT devices.

## ACKNOWLEDGMENT

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## APPENDIX: IMPACT OF GALLIUM NITRIDE-DIAMOND INTERFACE RESISTANCE ON THE CHANNEL TEMPERATURE

We perform finite-element analysis using COMSOL Multiphysics to investigate the role played by the GaN-diamond thermal interface resistance in the device channel temperature rise of the overall HEMT package, including the AlGaN/GaN epilayer, diamond substrate, and diamond microchannel. A device schematic for the simulation considers two thermal resistance mechanisms: i) conduction/spreading in GaN-on-diamond composite substrates (near-junction thermal transport, NJTT) and ii) fluidic convection in diamond microchannels (thermal transport in advanced heat sinks). The assumed microchannel features have a <100 μm width and an

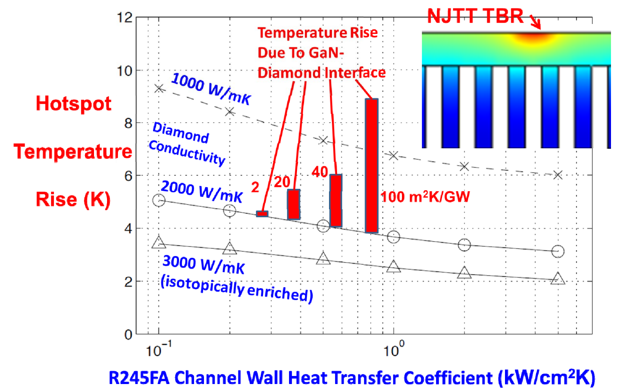


Fig. 3. Device channel temperature rise due to GaN-diamond thermal interface resistance, diamond substrate thermal conductivity, and convective resistance of cooling solution.

aspect ratio of 10:1. The 3-D conduction simulation dissipates a 5 kW cm$^{-2}$ in a device-level hot spot (200 µm x 200 µm) and 1 kW cm$^{-2}$ in the background (5 mm x 5 mm). Figure 3 depicts the results of the channel temperature rise for different diamond thermal conductivities and different values of the channel wall heat transfer coefficient. For example, a simulation result indicates that the hot spot temperature rise is 4.5 °C for a heat transfer coefficient of 10$^{-1}$ kW cm$^{-2}$ K$^{-1}$ and a diamond thermal conductivity of 2000 W m$^{-1}$ K$^{-1}$. The temperature rise due to the GaN-diamond thermal interface resistance is particularly important, as clearly indicated by red bars in Fig. 3. The large interface resistance of 100 m$^2$ K GW$^{-1}$ can account for more than 50% of the overall channel temperature rise when the diamond thermal conductivity is 2000 W m$^{-1}$ K$^{-1}$. The accurate determination of the GaN-diamond thermal interface resistance is therefore important for accurate prediction of the channel temperature rise.

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